■ GENERAL DESCRIPTION

■ PACKAGE OUTLINE

The **NJM2230** discriminate existance and fineness of video signal. It is applicable VCR, TV, Video camera, Hi-Fi VCR, on screen display and others.

FEATURES

- Operating Voltage
 - (+4.7V to + 13V) DMP8
- Package OutlineBipolar Technology

■ RECOMMENDED OPERATING CONDITION

• Operating Voltage V⁺=4.75 to 10V

■ APPLICATION

• Video camera, other video equipment

PIN CONFIGURATION

PIN FUNCTION

- 1. M.M Time Constant Set
- 2. SYNC Input (Comp, H, V SYNC)
- 3. SYNC Output
- 4. SSG SYNC Input
- 5. GND
- 6. SYNC DET, Judgement Control
- 7. M.M Smoothing 8. V⁺ 5~10V



NJM2230M

| ■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C | | | | |
|-------------------------------------|------------------|-------------|------|--|
| PARAMETER | SYMBOL | RATINGS | UNIT | |
| Supply Voltage | V^{+} | 12 | V | |
| Power Dissipation | PD | (DMP8) 300 | mW | |
| Operating Temperature Range | T _{opr} | -40 to +85 | O° | |
| Storage Temperature Range | T _{stg} | -40 to +125 | °C | |

■ FLECTRICAL CHARACTERISTICS

| ELECTRICAL CHARACTERISTICS (V ⁺ =5V, Ta=25 | | | | | a=25°C) | | |
|---|--------|----------------------------------|----------------|------|---------|------|------|
| PARAMETER | | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
| Operating Current | | lcc | | - | 8 | 11 | mA |
| Schmitt Circuit CAP Voltage | H side | V _{CAP-H} | (Note 1) | 2.07 | 2.22 | 2.37 | V |
| | Lside | V _{CAP-L} | (Note 1) | 1.57 | 1.72 | 1.87 | V |
| Schmitt Circuit LOCK Voltage | H side | V _{LOCK-H} | (Note 1) | 2.53 | 2.68 | 2.83 | V |
| | Lside | V _{LOCK-L} | (Note 1) | 1.25 | 1.40 | 1.55 | V |
| Mono-Multi Output Width | | W _{MM} | (Note 2) | - | 25 | - | µsec |
| | 2P | V _{TH-2} | | 1.0 | 1.5 | 2.0 | V |
| Input Threshold Level | 4P | V _{TH4} | | 1.0 | 1.5 | 2.0 | V |
| | 6P | V _{TH-6} | | - | 0.8 | 1.4 | V |
| | H side | V _{7-H} | | 4.9 | 5.0 | - | V |
| Output Voltage Pin 7 | Lside | V _{7-L} | | - | 0.1 | 0.3 | V |
| Output Voltage Pin 6 | H side | V _{6-H} | | 3.6 | 4.0 | - | V |
| | Lside | V _{6-L} | | - | - | 0.1 | V |
| Output Voltage Pin 3 | H side | V _{3-H} | | 4.9 | 5.0 | - | V |
| | Lside | V _{3-L} | | - | 0.1 | 0.3 | V |
| M. M Smoothed D.C. Voltage | • | V ₈ (V ₇) | Pin 2=2V | 2.9 | 3.2 | 3.5 | V |

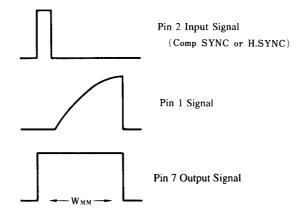
NJM2230

(Note 1) 5V VLOCK-H VCAP-H VCAP-H VCAP-L VLOCK-L 0 V Capture Range Lock Range

| | ITEM | V _{CAP-L} | V _{LOCK-H} | V _{CAP-H} | V _{LOCK-L} |
|---|---------------|--------------------|---------------------|--------------------|---------------------|
| Ī | Pin 7 Voltage | 0 — | | 5 — | → 0 |
| | Pin 6 Voltage | L | Н —► | L — 🕨 H | 1 → L |

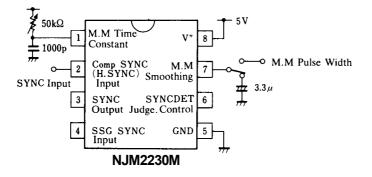
Measure Pin 7 Voltage at a moment when Pin 6 output voltage turns state.



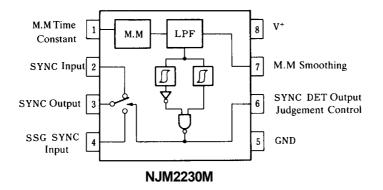


Adjust Pin 7 DC Voltage to 2V (at $V^+=5V$) by varying Pin 1 outer resistor, and test Pin7 output pulse width after taking off Pin7 outer capacitor.

■ TEST CIRCUIT



■ OPERATIVE PRINCIPLE

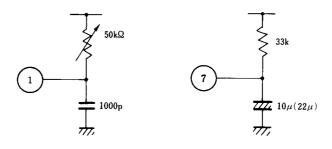


- M. M: Varies duty ratio of output signal depended on input synchronous signal condition (irregular, on, signal)
- LPF: Converss M. M. output signal to DC level. The more larger the duty ratio is, DC level is clamped at $V^+/2+0.7$ (V).
- Comparator: Outputs discriminating signal of input signal by DC level of LPF output. Stablized output signal can be obtained due to that the hysterises is given to the output.
- Switch Makes exchanging operation of SYNC Input and SSG SYNC Input signal by discriminating signal from comparator or Pin 6 signal of SYNC DET Output Judgement Control.

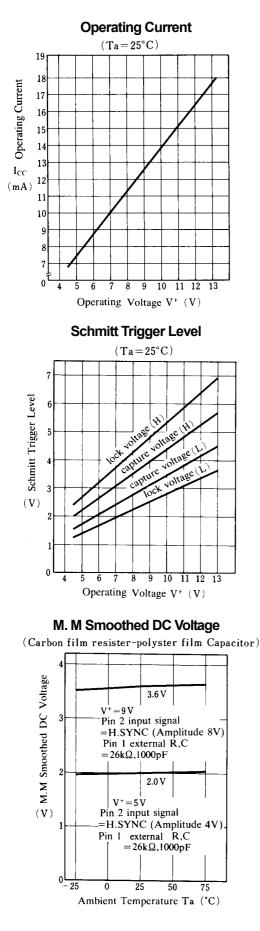
TERMINAL FUNCTION

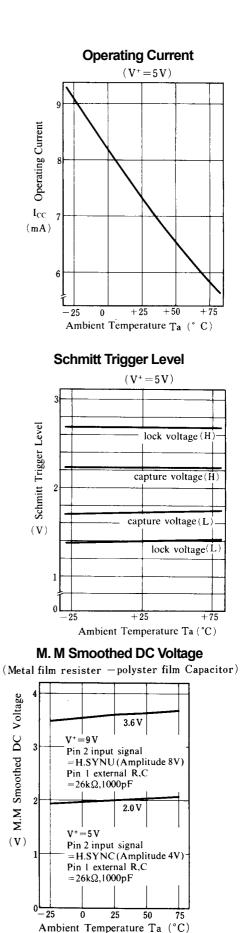
| PIN NO. | EXPLANATION |
|---------|--|
| 1 | Connect resistor and capacitor for M. M. time constant. (Value of R, C is changed by a kind of Pin 2 SYNC Input siganal.) |
| 2 | Input synchronous signal (Comp SYNC, H. SYNC or V. SYNC) separated from video signal. |
| 3 | It outputs Pin 2 or Pin 4 signal by Pin 2 signal condition. ● Pin 2 input signal; normal → Output Pin 2 input signal. ● Pin 2 input signal; abnormal → Output Pin 4 input signal. |
| 4 | Input artifical synchronous signal generated by SSG (Sync. Signal Generator). |
| 5 | GND |
| 6 | Input DC voltage (H or L state) by Pin 2 signal condition. When outer SW is turned to 1, Pin 2 input signal is forced to flow out from Pin 3. Pin 2 input signal; normal → H state Pin 2 input signal; abnormal → L state |
| 7 | Connect capacitor for smoothing M. M. (Value depends on Pin 2 input Signal). Adjust Pin 1 attached volume to the level that Pin 8 voltage becomes 2V (V ⁺ =5V) with Pin 2 signal. If V ⁺ >5V, then V ₇ =2/5V ⁺ (V) |
| 8 | V ⁺ : 5 to 10V |

(Note) In some application, it happens that still, search or tracking is large off the point and unordinaryh SYNC of SYNC occurs. If it is not desirable, you can do in SYNC condition by using Pin 6 as control input terminal. Also recommend sensitivity adjustment of outer device change, by it error detection of unodinary SYNC will lapse. It makes volume to low value, in other word it makes time constant of M. M. to low value. In this case synchronous peak voltage at Pin 7 becomes lower and so makes to 2V (V⁺=5V) by putting resistor in to V⁺. (Adjust to 2V by Pin 1 resistor attached.)



TYPICAL CHARACTERISTICS





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